REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-26 are pending. Claims 1-26 are rejected. Claims 1, 8, 14, and 21 have been amended. Claims 3, 10, 13, 16, and 23 have been cancelled.

Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter.

Claim Objections

Claim 13 has been objected to because it is an exact repetition of claim 12.

Claim 13 has been cancelled to overcome the Examiner's objection.

Rejections Under 35 U.S.C. § 102

Claims 1, 4, 5, 8, 11, 14, 17, 18, 21 and 24 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by U.S. Patent No. 5,920,219 of Young, et al, ("Young").

Young discloses a clock-controlled precision monostable circuit that generates output pulses having the duration controlled by the pulse width of the clock signal. The parts of the reference cited by the Examiner state that

> ...clock generator), and configuring the monostable circuit such that its output pulse duration is essentially an exclusive function of the pulse width (or duration between successive, opposite-going transitions) of the precision clock signal.

(Col. 1, lines 40-44) (emphasis added)

and that

> As described above, a significant feature of each of the pulse duration control circuit 20 and monostable circuit arrangement 10 is the fact that their operation is effectively independent of variations in parameters of the components of which the circuits are configured and instead are dependent only upon the pulse width of the clock signal CLK BAR, which can be established very precisely with state of...

(Col. 4, lines 9-15)

Young, however, also discloses that the output pulse is generated by the input signal, which is different from the clock signal. More specifically, Young states

> The clock signal-controlled, precision pulse generator circuit in accordance with the present invention is schematically illustrated in FIG.1, as comprising a multivibrator circuit arrangement 10 having an input terminal 12 to which an input signal(S) is applied, and an output terminal 14 from which an output pulse is produced in response to the application of the input signal (S) to the input terminal 12. Multivibrator circuit arrangement 10 further includes a control terminal 16, which is coupled to receive a pulse duration control voltage generated by a pulse duration control circuit 20. Pulse duration control circuit 20 has an input terminal 22, to which a clock signal CLK BAR is applied, and is operative to assert a control voltage to the control terminal 16 of multivibrator circuit 10, in accordance with the pulse width of the precision clock signal CLK BAT applied to the input terminal 22 of the pulse duration control circuit 20, as will be described

(Col.3, lines 59-65) (emphasis added)

In particular, Young discloses that

> As a consequence, over multiple clock cycles, the pulse duration circuit 20 operates to bring the amount of charge stored on reference storage capacitor 110 to a stable value, such that the length of time required to discharge capacitor 112 from its fully charged value to the reference value VR is exactly equal to the duration of one-half a clock cycle (namely, between successive opposite-going transitions of the clock signal). In the timing diagrams of FIG. 2, this means that the point in time that capacitor 112 is discharged by current source FET 80 to the value VR coincides with edge 37-2 of the output of flip-flop 30.
>
> Namely, once the circuit has stabilized, the time at which discharge voltage reduction segment 112-1 in timing diagram 2 reaches the threshold reference VR will be coincident with high-to-low edge 37-2 of the output of flip-flop 30 (which tracks the clock signal CLK BAR), whereby making the voltage across voltage reference capacitor 110 proportional to the pulse width of the controlling clock signal. As detailed below in connection with the discription of the operation of multivibrator circuit arrangement 10, this clock signal pulse width dependent reference voltage serves as a precision control voltage for setting the pulse duration of the output of the monostable multivibrator 10.

(Young, col. 8, lines 30-52) (emphasis added)

In contrast to the presently claimed invention, Young merely discloses a circuit that generates output pulses in response to the input signal, which is different from the clock signal, wherein the duration of the output pulses is controlled by the clock signal. Young does not

disclose a circuit that generates an output phase synchronized to an input clock signal at a predetermined time, which is delayed in respect to the input clock signal, and which is dependent on a ratio of capacitance values and on a logic phase width of the clock signal and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance, as recited in amended independent claim 1 given below:

> An apparatus comprising:
>
> a circuit configured to receive an input clock signal and to generate an output phase synchronized to said input clock signal at a predetermined time delayed relative to said input clock signal, wherein the predetermined time is dependent on a logic phase width of said input clock signal and on a ratio of capacitance values and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance.

(emphasis added)

Because Young does not set forth all the limitations of amended claim 1, Applicant respectfully submits that amended claim 1 is not anticipated by Young under 35 U.S.C. §102(b).

Given that claims 2 and 4-7 depend, directly or indirectly on amended claim 1, and contain at least the same limitations as amended claim 1, Applicant respectfully submits that claims 2 and 4-7 are likewise not anticipated by Young under 35 U.S.C. §102(b).

Given that amended claims 8, 14, and 21 contain at least the same limitations as amended claim 1, Applicant respectfully submits that amended claims 8, 14, and 21 are likewise not anticipated by Young under 35 U.S.C. §102(b).

Given that claims 9, 11, 12, 15, 17- 20, 22, and 24-26 depend, directly or indirectly on respective amended claims 8, 14, and 21, and contain at least the same limitations as amended claims 8, 14, and 21, Applicant respectfully submits that claims 9, 11, 12, 15, 17- 20, 22 and 24-26 are likewise not anticipated by Young under 35 U.S.C. §102(b).

Rejections Under 35 U.S.C. § 103(a)

Claims 2, 6, 7, 9, 12, 13, 15, 19, 20, 22, 25 and 26 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,920,219 of Young, et al, ("Young").

Claims 3, 10, 16 and 23 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,920,219 of Young, et al ("Young") in view of U.S. Patent No. 5,578,952 of Shoji ("Shoji").

With respect to amended claim 1, as discussed above, Young fails to disclose a circuit that generates an output phase synchronized to an input clock signal at a predetermined time, which is delayed in respect to the input clock signal, and which is dependent on a ratio of capacitance values and on a logic phase width of the clock signal and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance.

Similarly, Shoji also fails to disclose a circuit that generates an output phase synchronized to an input clock signal at a predetermined time, which is delayed in respect to the input clock signal, and which is dependent on a ratio of capacitance values and on a logic phase width of the clock signal and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance, as recited in amended claim 1.

Shoji discloses a fixed-interval timing circuit and method. The part of the reference cited by the Examiner states that

> Instead, the circuit of FIG. 1 provides a fixed duration pulse or delay as a function of the ratio of the value of reference capacitor 114 (C_{ref}) and delay capacitor 115 (C_{delay})--While typical integrated circuit fabrication methods make precise control of absolute device values difficult, the relative device values upon the wafer can be accurately maintained.

(Col. 2, lines 44-50)

Similar to Young, Shoji discloses that the output is synchronized with the trigger signal, and is not synchronized with a clock signal. More specifically Shoji states

> To initiate the operation of the circuit illustrated in FIGS. 1 and 3, the trigger signal applied to terminal 126 is brought from a logical 0 state to a logical 1 state (shown to occur at time t_0 in FIG. 2). In order to ensure a reliable output by the circuit of FIGS. 1 and 3 the particular instant at which the trigger signal makes the transition need not be synchronized with respect to any transition in signal level by the reference clock, or the signal evident at node 122. Furthermore, the period over which the trigger signal is held in a logical 1 state ($t_f - t_0$ as shown by waveform 204 in FIG. 2) is also inconsequential with respect to the generation of fixed time signal or delay by the circuit (except for the obvious limitation that the interval $t_f - t_0$ have a longer duration than T_{fix}, the signal that will be output by the circuit of FIGS. 1 and 3 at terminal 132).

(Shoji, col. 3, lines 46-61) (emphasis added)

Further, Shoji discloses that a fixed delay is defined as a sum of the time duration and the total delay introduced by other elements of the circuit. In particular, Shoji discloses

> The fixed duration, T_{fix}, of the signal provided by the circuit illustrated in FIGS. 1 and 3 is the time from t_2 to time t_4, and can be defined as the time it takes for the voltage at node 127 to decay from V_{DD} to V_{th}, and can be represented as:
> $T_{fix} = (C_{delay} / 8C_{ref} f_c) (-\ln (V_{th} / V_{DD}))$
>
> As V_{DD}, V_{th}, and f_c are known, fixed values, the only true variable in determining the duration of T_{fix} is C_{ref}/C_{delay}. As standard integrated circuit fabrication techniques allow relative device characteristics to be held to tight tolerances, the circuitry of FIG. 1, when implemented upon an integrated circuit, will reliably and accurately provide a signal defining a fixed interval.
>
> The invention illustrated in FIGS. 1 and 3 can also be utilized to provide a fixed delay. The trailing edge of the pulse in waveform 206 (FIG. 2) will always be delayed by exactly (T_{fix} +K) from time t_0 (the time at which the trigger signal made the transition from logical 0 to logical 1). K is the total delay introduced by the operation of low-pass comparator 129, buffers 111-113, and inverters 109 and 110. K is a constant for a particular circuit, and can be readily computed (based upon the physical characteristics of the particular devices in the circuit) or measured.

(Shoji, col. 4, lines 33-58) (emphasis added)

Unlike the presently claimed invention, Shoji discloses that output pulses are synchronized with a trigger signal, and not with the clock signal. Moreover, unlike the presently

claimed invention, Shoji discloses that a fixed delay of the output pulses is merely defined as a sum of the fixed pulse duration and the total delay introduced by the operation of other elements in the circuit.

Hence, neither Young nor Shoji discloses, teaches, or suggests a circuit that generates an output phase synchronized to an input clock signal at a predetermined time, which is delayed in respect to the input clock signal, and which is dependent on a ratio of capacitance values and on a logic phase width of the clock signal and is independent of at least one of the process parameters including transistor drive current, parasitic resistance, and parasitic capacitance, as recited in amended claim 1.

Consequently, even if Young and Shoji were combined, such a combination would lack the limitation of amended claim 1.

Therefore, Applicant respectfully submits that amended claim 1 is not obvious under 35 U.S.C. §103(a) over Young, in view of Shoji.

Given that claims 2 and 4-7 depend on amended claim 1, directly or indirectly, and add additional limitations, Applicant respectfully submits that claims 2 and 4-7 are likewise not obvious under 35 U.S.C. §103(a) over Young, in view of Shoji.

Given that amended claims 8, 14, and 21 contain at least the same limitations as amended claim 1, Applicant respectfully submits that amended claims 8, 14, and 21 are likewise not obvious under 35 U.S.C. §103(a) over Young, in view of Shoji.

Given that claims 9, 11, 12, 15, 17- 20, 22, and 24-26 depend, directly or indirectly on respective amended claims 8, 14, and 21, and contain at least the same limitations as amended claims 8, 14, and 21, Applicant respectfully submits that claims 9, 11, 12, 15, 17- 20, 22 and 24-26 are likewise not obvious under 35 U.S.C. §103(a) over Young, in view of Shoji.

In conclusion, Applicant respectfully submits that in view of the arguments and amendments set forth herein, the applicable rejections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Michael Mallie at (408) 720-8300. If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

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